



Product Change Notification - SYST-12NNJX959

Date:

15 Jul 2019

Product Category:

32-bit Microcontrollers; Tolerant Devices

Affected CPNs:**Notification subject:**

ERRATA - SAM E70/S70/V70/V71 Family Errata and Data Sheet Clarification

Notification text:

SYST-12NNJX959

Microchip has released a new DeviceDoc for the SAM E70/S70V70/V71 Family Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [SAM E70/S70V70/V71 Family Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change:

- 1) Updated the Silicon Issue Summary table to be more readable.
- 2) The following Silicon Issues were updated:
 - a) Boundary Scan Mode: Internal Regulator
 - b) XDMAC: TCM Accesses
 - c) FFPI: Flash Programming
 - d) PMC: Wait Mode Exit Fail from Flash
 - e) SDRAMC: SDRAM Controller Scrambling Use Limitation
 - f) SMC: SMC_WPSR Register Write Protection
 - g) TWIHS: I²C Hold Timing Incompatibility
 - h) TWIHS: Clear Command
- 3) The following Silicon Issues were added:
 - a) DEVICE: System Performance
 - b) SDRAMC: Operational Voltage

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 15 July 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

[SAM E70/S70V70/V71 Family Errata and Data Sheet Clarification](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

Terms and Conditions:



If you wish to receive Microchip PCNs via email please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

ATSAME70-XPLD
ATSAME70J19A-AN
ATSAME70J19A-ANT
ATSAME70J20A-AN
ATSAME70J20A-ANT
ATSAME70J20B-AN
ATSAME70J20B-ANT
ATSAME70J21A-AN
ATSAME70J21A-ANT
ATSAME70J21B-AN
ATSAME70J21B-ANT
ATSAME70N19A-AN
ATSAME70N19A-ANT
ATSAME70N19A-CN
ATSAME70N19A-CNT
ATSAME70N19B-AN
ATSAME70N19B-ANT
ATSAME70N19B-CN
ATSAME70N19B-CNT
ATSAME70N20A-AN
ATSAME70N20A-ANT
ATSAME70N20A-CN
ATSAME70N20A-CNT
ATSAME70N20A-CUN01
ATSAME70N20B-AN
ATSAME70N20B-ANT
ATSAME70N20B-CN
ATSAME70N20B-CNT
ATSAME70N20B-CUN01
ATSAME70N21A-AN
ATSAME70N21A-ANT
ATSAME70N21A-CN
ATSAME70N21A-CNT
ATSAME70N21B-AN
ATSAME70N21B-ANT
ATSAME70N21B-CN
ATSAME70N21B-CNT
ATSAME70Q19A-AN
ATSAME70Q19A-ANT
ATSAME70Q19A-CFN
ATSAME70Q19A-CFNT
ATSAME70Q19A-CN
ATSAME70Q19A-CNT
ATSAME70Q19B-AN
ATSAME70Q19B-ANT
ATSAME70Q19B-CFN

ATSAME70Q19B-CFNT
ATSAME70Q19B-CN
ATSAME70Q19B-CNT
ATSAME70Q20A-AN
ATSAME70Q20A-ANT
ATSAME70Q20A-CFN
ATSAME70Q20A-CFNT
ATSAME70Q20A-CN
ATSAME70Q20A-CNT
ATSAME70Q20B-AN
ATSAME70Q20B-ANT
ATSAME70Q20B-CFN
ATSAME70Q20B-CFNT
ATSAME70Q20B-CN
ATSAME70Q20B-CNT
ATSAME70Q21A-AN
ATSAME70Q21A-ANT
ATSAME70Q21A-CFN
ATSAME70Q21A-CFNT
ATSAME70Q21A-CN
ATSAME70Q21A-CNT
ATSAME70Q21B-AN
ATSAME70Q21B-ANT
ATSAME70Q21B-CFN
ATSAME70Q21B-CFNT
ATSAME70Q21B-CN
ATSAME70Q21B-CNT
ATSAMS70J19A-AN
ATSAMS70J19A-ANT
ATSAMS70J19A-MN
ATSAMS70J19A-MNT
ATSAMS70J20A-AN
ATSAMS70J20A-ANT
ATSAMS70J20A-MN
ATSAMS70J20A-MNT
ATSAMS70J20B-AN
ATSAMS70J20B-ANT
ATSAMS70J20B-MN
ATSAMS70J20B-MNT
ATSAMS70J21A-AN
ATSAMS70J21A-ANT
ATSAMS70J21A-MN
ATSAMS70J21A-MNT
ATSAMS70J21B-AN
ATSAMS70J21B-ANT
ATSAMS70J21B-MN
ATSAMS70J21B-MNT
ATSAMS70N19A-AN
ATSAMS70N19A-ANT

ATSAMS70N19A-CFN
ATSAMS70N19A-CFNT
ATSAMS70N19A-CN
ATSAMS70N19A-CNT
ATSAMS70N19B-AN
ATSAMS70N19B-ANT
ATSAMS70N19B-CFN
ATSAMS70N19B-CFNT
ATSAMS70N19B-CN
ATSAMS70N19B-CNT
ATSAMS70N20A-AN
ATSAMS70N20A-ANT
ATSAMS70N20A-CFN
ATSAMS70N20A-CFNT
ATSAMS70N20A-CN
ATSAMS70N20A-CNT
ATSAMS70N20B-AN
ATSAMS70N20B-ANT
ATSAMS70N20B-CFN
ATSAMS70N20B-CFNT
ATSAMS70N20B-CN
ATSAMS70N20B-CNT
ATSAMS70N21A-AN
ATSAMS70N21A-ANT
ATSAMS70N21A-CFN
ATSAMS70N21A-CFNT
ATSAMS70N21A-CN
ATSAMS70N21A-CNT
ATSAMS70N21B-AN
ATSAMS70N21B-ANT
ATSAMS70N21B-CFN
ATSAMS70N21B-CFNT
ATSAMS70N21B-CN
ATSAMS70N21B-CNT
ATSAMS70Q19A-AN
ATSAMS70Q19A-AN-101
ATSAMS70Q19A-ANT
ATSAMS70Q19A-CFN
ATSAMS70Q19A-CFNT
ATSAMS70Q19A-CN
ATSAMS70Q19A-CNT
ATSAMS70Q19B-AN
ATSAMS70Q19B-ANT
ATSAMS70Q19B-CFN
ATSAMS70Q19B-CFNT
ATSAMS70Q19B-CN
ATSAMS70Q19B-CNT
ATSAMS70Q20A-AN
ATSAMS70Q20A-ANT

ATSAMS70Q20A-CFN
ATSAMS70Q20A-CFNT
ATSAMS70Q20A-CN
ATSAMS70Q20A-CNT
ATSAMS70Q20B-AN
ATSAMS70Q20B-ANT
ATSAMS70Q20B-CFN
ATSAMS70Q20B-CFNT
ATSAMS70Q20B-CN
ATSAMS70Q20B-CNT
ATSAMS70Q21A-AN
ATSAMS70Q21A-ANT
ATSAMS70Q21A-CFN
ATSAMS70Q21A-CFNT
ATSAMS70Q21A-CN
ATSAMS70Q21A-CNT
ATSAMS70Q21B-AN
ATSAMS70Q21B-ANT
ATSAMS70Q21B-CFN
ATSAMS70Q21B-CFNT
ATSAMS70Q21B-CN
ATSAMS70Q21B-CNT
ATSAMV70J19B-AAB
ATSAMV70J19B-AABT
ATSAMV70J20B-AAB
ATSAMV70J20B-AABT
ATSAMV70N19B-AAB
ATSAMV70N19B-AABT
ATSAMV70N19B-CB
ATSAMV70N19B-CBT
ATSAMV70N20A-CBT
ATSAMV70N20B-AAB
ATSAMV70N20B-AABT
ATSAMV70N20B-CB
ATSAMV70N20B-CBT
ATSAMV70N20B-CBTV08
ATSAMV70N20B-CBTV12
ATSAMV70Q19B-AAB
ATSAMV70Q19B-AABT
ATSAMV70Q19B-AABTV07
ATSAMV70Q19B-CB
ATSAMV70Q19B-CBT
ATSAMV70Q19B-CBTV01
ATSAMV70Q19B-CBTVAO
ATSAMV70Q20B-AAB
ATSAMV70Q20B-AABT
ATSAMV70Q20B-AABTV10
ATSAMV70Q20B-CB
ATSAMV70Q20B-CBT

ATSAMV70Q20B-CBTVAO
ATSAMV70Q20B-CBVAO
ATSAMV71-XULT
ATSAMV71J19B-AAB
ATSAMV71J19B-AABT
ATSAMV71J20B-AAB
ATSAMV71J20B-AABT
ATSAMV71J21B-AAB
ATSAMV71J21B-AAB-ES2
ATSAMV71J21B-AABT
ATSAMV71J21B-AABTV16
ATSAMV71J21B-AABTVAO
ATSAMV71N19B-AAB
ATSAMV71N19B-AABT
ATSAMV71N19B-AABTV04
ATSAMV71N19B-CB
ATSAMV71N19B-CBT
ATSAMV71N20B-AAB
ATSAMV71N20B-AABT
ATSAMV71N20B-AABV14
ATSAMV71N20B-CB
ATSAMV71N20B-CBT
ATSAMV71N20B-CBTV03
ATSAMV71N21B-AAB
ATSAMV71N21B-AABT
ATSAMV71N21B-CB
ATSAMV71N21B-CBT
ATSAMV71N21B-CBTV02
ATSAMV71N21B-CBTV09
ATSAMV71N21B-CBTV15
ATSAMV71N21B-CBV06
ATSAMV71N21B-CBV11
ATSAMV71Q19B-AAB
ATSAMV71Q19B-AABT
ATSAMV71Q19B-CB
ATSAMV71Q19B-CBT
ATSAMV71Q20B-AAB
ATSAMV71Q20B-AABT
ATSAMV71Q20B-CB
ATSAMV71Q20B-CBT
ATSAMV71Q21B-AAB
ATSAMV71Q21B-AABT
ATSAMV71Q21B-AABTV13
ATSAMV71Q21B-CB
ATSAMV71Q21B-CBT
ATSAMV71Q21B-CBTV05
SAMV71Q21ET-H8X-HP
SAMV71Q21RT-DHB-E
SAMV71Q21RT-DHB-GRC

SAMV71Q21RT-DHB-MQ
SAMV71Q21RT-DHB-SV
SAMV71Q21RT-H8X-ENG
SAMV71Q21RT-H8X-HP
SAMV71Q21RT-H8X-SN



SAM E70/S70/V70/V71 Family

SAM E70/S70/V70/V71 Family Silicon Errata and Data Sheet Clarification

SAM E70/S70/V70/V71 Family

The SAM E70/S70/V70/V71 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001527C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in [1. Silicon Issue Summary](#).

The errata described in this document will be addressed in future revisions of the SAM E70/S70/V70/V71 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in [23. Data Sheet Clarifications](#), following the discussion of silicon issues.

The Device and Revision ID values for the various SAM E70/S70/V70/V71 family silicon revisions are shown in the following tables.

Table 1. SAM V71 Silicon Device Identification

Part Number	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHIPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAMV71Q19	0xA12D_0A0x	0x00000002	0x0	0x1
SAMV71Q20	0xA122_0C0x	0x00000002		
SAMV71Q21	0xA122_0E0x	0x00000002		
SAMV71N19	0xA12D_0A0x	0x00000001		
SAMV71N20	0xA122_0C0x	0x00000001		
SAMV71N21	0xA122_0E0x	0x00000001		
SAMV71J19	0xA12D_0A0x	0x00000000		
SAMV71J20	0xA122_0C0x	0x00000000		
SAMV71J21	0xA122_0E0x	0x00000000		

Table 2. SAM V70 Silicon Device Identification

Part Number	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHIPID_CIDR[31:0]]	CHIPID_EXID[31:0]]	A	B
SAMV70Q19	0xA13D_0A0x	0x00000002	0x0	0x1
SAMV70Q20	0xA132_0C0x	0x00000002		
SAMV70N19	0xA13D_0A0x	0x00000001		
SAMV70N20	0xA132_0C0x	0x00000001		
SAMV70J19	0xA13D_0A0x	0x00000000		
SAMV70J20	0xA132_0C0x	0x00000000		

Table 3. SAM S70 Silicon Device Identification

Part Number	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHIPID_CIDR[31:0]]	CHIPID_EXID[31:0]]	A	B
SAMS70Q19	0xA11D_0A0x	0x00000002	0x0	0x1
SAMS70Q20	0xA112_0C0x	0x00000002		
SAMS70Q21	0xA112_0E0x	0x00000002		
SAMS70N19	0xA11D_0A0x	0x00000001		
SAMS70N20	0xA112_0C0x	0x00000001		
SAMS70N21	0xA112_0E0x	0x00000001		
SAMS70J19	0xA11D_0A0x	0x00000000		
SAMS70J20	0xA112_0C0x	0x00000000		
SAMS70J21	0xA112_0E0x	0x00000000		

Table 4. SAM E70 Silicon Device Identification

Part Number	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHIPID_CIDR[31:0]]	CHIPID_EXID[31:0]]	A	B
SAME70Q19	0xA10D_0A0x	0x00000002	0x0	0x1
SAME70Q20	0xA102_0C0x	0x00000002		
SAME70Q21	0xA102_0E0x	0x00000002		
SAME70N19	0xA10D_0A0x	0x00000001		
SAME70N20	0xA102_0C0x	0x00000001		
SAME70N21	0xA102_0E0x	0x00000001		
SAME70J19	0xA10D_0A0x	0x00000000		
SAME70J20	0xA102_0C0x	0x00000000		
SAME70J21	0xA102_0E0x	0x00000000		

Note:

1. Refer to the “Chip Identifier (CHIPID)” section in the current Device Data Sheet (DS60001527C) for detailed information on Chip Identification and Revision IDs for your specific device.

Table of Contents

SAM E70/S70/V70/V71 Family.....	1
1. Silicon Issue Summary.....	7
2. Analog Front-End Controller (AFEC).....	10
2.1. Write Protection Reference: M32DOC-497.....	10
2.2. Performance Reference: M32DOC-498.....	10
2.3. AOFF bit Reference: TPUBSAMV-35.....	10
3. ARM Cortex-M7.....	12
3.1. ARM® Cortex®-M7 Reference: M32DOC-499.....	12
4. Boundary Scan Mode.....	13
4.1. Internal Regulator Reference: M32DOC-500.....	13
5. Device.....	14
5.1. AHB Peripheral (AHBP) Port Frequency Ratio Reference: M32DOC-501.....	14
5.2. AHB Slave (AHBS) Port Latency Access Reference: M32DOC-502.....	14
5.3. System Performance Reference: M32S-221.....	14
6. Extended DMA Controller (XDMAC).....	16
6.1. TCM Accesses Reference: M32DOC-503.....	16
6.2. Byte and Half-Word Accesses Reference: M32DOC-506.....	16
6.3. Request Overflow Error Reference: M32DOC-509.....	16
7. Fast Flash Programming Interface (FFPI).....	17
7.1. Flash Programming Reference: M32DOC-510.....	17
8. Ethernet MAC (GMAC).....	18
8.1. Priority Queues Reference: M32DOC-535.....	18
9. Inter-IC Sound Controller (I2SC).....	19
9.1. Module Availability Reference: M32DOC-515.....	19
9.2. Corrupted First Sent Data Reference: M32DOC-516.....	19
10. Controller Area Network (MCAN).....	20
10.1. Non-ISO Operation Reference: M32DOC-536.....	20
10.2. MCAN_CCCR Register Reference: M32DOC-537.....	20
10.3. Transmitter Delay Compensation Value (TDCV) Bits Reference: M32DOC-538.....	20
10.4. MCAN_PSR Register Reference: M32DOC-539.....	21
10.5. MCAN_IR Register Reference: M32DOC-540.....	21
10.6. MCAN_IE Register Reference: M32DOC-541.....	21
10.7. MCAN_ILS Register Reference: M32DOC-542.....	22
10.8. MCAN Data Bit Timing and Prescaler Register Reference: M32DOC-543.....	22
10.9. MCAN Nominal Bit Timing and Prescaler Register Reference: M32DOC-544.....	22
10.10. MCAN Transmitter Delay Compensation Register Reference: M32DOC-545.....	23

10.11. Timestamping Function Reference: M32DOC-546.....	23
11. Parallel Input/Output (PIO).....	24
11.1. PIO Line Configuration for AFEC and DACC Analog Inputs Reference: MC32DOC-517.....	24
12. Power Management Controller (PMC).....	25
12.1. Wait Mode Exit Fail from Flash Reference: M32DOC-518.....	25
12.2. PMC_OCR Register Calibration Reporting Reference: M32DOC-519.....	25
13. Quad Serial Peripheral Interface (QSPI).....	26
13.1. Module Hangs with Long DLYCS Reference: M32DOC-520.....	26
13.2. WDRBT Reference: M32DOC-592.....	26
14. Real-Time Clock (RTC).....	27
14.1. RTC_CALR Reset Value Reference: M32DOC-521.....	27
15. SDRAM Controller (SDRAMC).....	28
15.1. SDRAM Controller Scrambling Use Limitation Reference: M32DOC-522.....	28
15.2. USB and SDRAM Concurrent Access Issue Reference: M32DOC-568.....	28
15.3. Operational Voltage Reference: M32S-200.....	28
16. Static Memory Controller (SMC).....	29
16.1. SMC_WPSR Register Write Protection Reference: M32DOC-523.....	29
17. Serial Synchronous Controller (SSC).....	30
17.1. Inverted Left/Right Channels Reference: M32DOC-524.....	30
17.2. Unexpected TD Output Delay Reference: M32DOC-525.....	30
18. Supply Controller (SUPC).....	31
18.1. Write-Protection Reference: M32DOC-526.....	31
18.2. Programmable Clock Controller Reference: M32VAL-5836.....	31
19. TWI High-Speed (TWIHS).....	32
19.1. I ² C Hold Timing Incompatibility Reference: M32DOC-527.....	32
19.2. Clear Command Reference: M32DOC-528.....	32
20. Universal Synchronous Asynchronous Receiver Transmitter (USART).....	33
20.1. Flow Control with DMA Reference: M32DOC-529.....	33
20.2. Bad Frame Detection Reference: M32DOC-530.....	33
21. USB High-Speed (USBHS).....	34
21.1. USBHS Host Does Not Function in Low-Speed Mode Reference: M32DOC-531.....	34
21.2. 64-pin LQFP Package Reference: M32DOC-532.....	34
21.3. NO DMA for Endpoint 7 Reference: M32DOC-533.....	34
22. Digital to Analog Converter Controller (DACC).....	35
22.1. Interpolation Mode Reference: BUG300.....	35

23. Data Sheet Clarifications.....	36
23.1. Controller Area Network (MCAN).....	36
23.2. Quad Serial Peripheral Interface (QSPI)	36
24. Appendix A: Revision History.....	37
The Microchip Web Site.....	38
Customer Change Notification Service.....	38
Customer Support.....	38
Microchip Devices Code Protection Feature.....	38
Legal Notice.....	39
Trademarks.....	39
Quality Management System Certified by DNV.....	40
Worldwide Sales and Service.....	41

SAM E70/S70/V70/V71 Family

Silicon Issue Summary

1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Feature	Errata Number	Summary	Affected Silicon Revisions	
				A	B
AFEC	Write Protection	2.1	The AFEC_CSELR register is not write-protected.	X	X
AFEC	Performance	2.2	The AFEC is sensitive to noise. Too much noise may lead to reduced AFEC performance, especially INL, DNL and SNR.	X	X
AFEC	AOFF bit	2.3	Changing the AOFF bit in the AFEC_COCCR register during conversions is not safe.	X	X
ARM Cortex-M7	ARM® Cortex®-M7	3.1	All issues related to the ARM r0p1 (for MRLA) and r1p1 (and MRLB) cores are described on the ARM site.	X	X
Boundary Scan Mode	Internal Regulator	4.1	The internal regulator is OFF in Boundary Scan mode.	X	
Device	AHB Peripheral (AHBP)	5.1	Peripheral accesses done through the AHBP with a Core/Bus ratio of 1/3 and 1/4 may lead to unpredictable results.	X	X
Device	AHB Slave (AHBS) Port Latency Access	5.2	DMA accesses done through the AHBS to the TCM with a Core/Bus ratio of 1/2, 1/3, and 1/4 may lead to latency due to one Wait state added to the access from the bus to AHBS.	X	X
Device	System Performance	5.3	Uncorrelated Noise and/or clock Jitter	X	X
XDMAC	TCM Accesses	6.1	If TCM accesses are generated through the AHBS port of the core, only 32-bit accesses are supported.	X	
XDMAC	Byte and Half-Word Accesses	6.2	If XDMAC is used to transfer 8-bit or 16-bit data in Fixed Source Address mode or Fixed Destination Address mode, source and destination addresses are incremented by 8-bit or 16-bit.	X	X
XDMAC	Request Overflow Error	6.3	When a DMA memory-to-memory transfer is performed, if the hardware request line selected by the field PERID bit in the XDMAC_CCx register toggles when the copy is enabled, the ROIS bit in the XDMAC_CISx register is set incorrectly.	X	X
FFPI	Flash Programming	7.1	The FFPI programs only 1 MB of Flash memory.	X	
GMAC	Priority Queues	8.1	On Revision A silicon, only three priority queues are available.	X	
I2SC	Module Availability	9.1	The Inter-IC Sound Controller (I2SC) is not available.	X	
I2SC	Corrupted First Sent Data	9.2	Immediately after the I2SC module is reset, the first data sent by the controller on the I2SDO line is corrupted.		X
MCAN	Non-ISO Operation	10.1	The default frame format on Revision A silicon does not match the default format specified in the current device data sheet.	X	
MCAN	MCANN_CCCR Register	10.2	In Revision A silicon, the MCAN CC Control register content does not match the content of the current device data sheet.	X	
MCAN	Transmitter Delay Compensation Value (TDCV) Bits	10.3	In Revision A silicon, the Transmitter Delay Compensation Value (TDCV) bit field does not match the content in the current device data sheet.	X	
MCAN	MCAN_PSR Register	10.4	In Revision A silicon, the content of the MCAN Protocol Status register differs from the content in the current device data sheet.	X	
MCAN	MCAN_IR Register	10.5	In Revision A silicon, the content of the MCAN Interrupt register differs from the content in the current device data sheet.	X	
MCAN	MCAN_IE Register	10.6	On Revision A silicon, the content in the MCAN Interrupt Enable register does not match the content in the current device data sheet.	X	
MCAN	MCAN_ILS Register	10.7	On Revision A silicon, the content in the MCAN Interrupt Line Support Register does not match the content in the current device data sheet.	X	

SAM E70/S70/V70/V71 Family

Silicon Issue Summary

.....continued

Module	Feature	Errata Number	Summary	Affected Silicon Revisions	
				A	B
MCAN	MCAN Data Bit Timing and Prescaler Register	10.8	On Revision A silicon, the MCAN Data Bit Timing and Prescaler register (MCAN_DBTP) is named MCAN Fast Bit Timing and Prescaler register (MCAN_FBTP).	X	
MCAN	MCAN Nominal Bit Timing and Prescaler Register	10.9	On Revision A silicon, the MCAN Nominal Bit Timing and Prescaler register (MCAN_NBTP) is named MCAN Bit Timing and Prescaler register (MCAN_BTP).	X	
MCAN	MCAN Transmitter Delay Compensation Register	10.10	In Revision A silicon, the MCAN Transmitter Delay Compensation Register (MCAN_TDCR) does not exist.	X	
MCAN	Timestamping Function	10.11	On Revision A silicon, TC Counter 0 is not connected to PCK6 and PCK7; therefore, the timestamping functionality does not exist.	X	
PIO	PIO Line Configuration for AFEC and DACC Analog Inputs	11.1	To enable the analog inputs, AFE_ADx or DACx, the pull-up resistors on the I/O lines must be disabled in the PIO user interface prior to writing registers AFEC_CHER or DACC_CHER.	X	X
PMC	Wait Mode Exit Fail from Flash	12.1	The delay to exit from Wait mode is too short to respect the Flash wake-up time from Stand-by mode and Deep Power-down mode. This delay may lead to bad opcode fetching.	X	X
PMC	PMC_OCR Register Calibration Reporting	12.2	When reading the PMC_OCR register with the SEL8 and SEL12 bits cleared, the CAL8 and CAL12 bits are not updated with the manufacturing calibration bits of the Main RC Oscillator. However, the Main RC Oscillator is loaded with this manufacturing calibration data.	X	X
QSPI	Module Hangs with Long DLYCS	13.1	The QSPI module hangs if a command is written to any QSPI register during the delay defined in the DLYCS bit. There is no status bit to flag the end of the delay.	X	X
QSPI	WDRBT	13.2	When the QSPI is in SPI mode, the WDRBT feature is not functional.	X	X
RTC	RTC_CALR Reset Value	14.1	On Revision A silicon, the reset value of the RTC_CALR register is 0x01E11220.	X	
SDRAMC	SDRAM Controller Scrambling Use Limitation	15.1	The scrambling/unsrambling feature of the SDRAM Controller (SDRAMC) has a use limitation.	X	
SDRAMC	USB and SDRAM Concurrent Access Issue	15.2	USB module functionality is adversely affected with concurrent SDRAM access.	X	X
SDRAMC	Operational Voltage	15.3	SDRAM operation not supported at 1.8Vdc.	X	X
SMC	SMC_WPSR Register Write Protection	16.1	When the write protection feature is enabled and a write attempt into a protected register is performed, the Write Protection Violation Source (WPVSR) bit field in the SMC_WPSR register does not report the right violation source.	X	X
SSC	Inverted Left/Right Channels	17.1	When the SSC is in Slave mode, the TF signal is derived from the codec and not controlled by the SSC.	X	
SSC	Unexpected TD Output Delay	17.2	An unexpected delay on TD output may occur when the SSC is configured under certain conditions.	X	X
SUPC	Write-Protection	18.1	The SUPC_WUIR register is not write-protected.	X	X
SUPC	Programmable Clock Controller Reference	18.2	Programmable Clock Outputs, PCK0–PCK2, selected from the clock generator outputs to drive the device PCK pins are not supported and should not be used.	X	X
TWIHS	I ² C Hold Timing Incompatibility	19.1	The TWIHS module is not compatible with I ² C hold timing.	X	
TWIHS	Clear Command	19.2	A bus reset using the CLEAR bit of the TWIHS Control register does not work correctly during a bus busy state.	X	
USART	Flow Control with DMA Reference	20.1	The RTS signal is not connected to the DMA. Therefore, when DMA is used, Flow Control is not supported.	X	X
USART	Bad Frame Detection	20.2	If a bad frame is received (i.e., incorrect baud rate) with the last data bit being sampled at 1, frame error detection does not occur.	X	X
USBHS	USBHS Host	21.1	The USB Host does not function in Low-Speed mode.	X	
USBHS	64-pin LQFP Package	21.2	The USBHS module does not function in 64-pin LQFP package devices.	X	X

SAM E70/S70/V70/V71 Family

Silicon Issue Summary

.....continued

Module	Feature	Errata Number	Summary	Affected Silicon Revisions	
				A	B
USBHS	NO DMA for Endpoint 7	21.3	The DMA feature is not available for Pipe/Endpoint 7.	X	X
DACC	Interpolation Mode	22.1	Interpolation Mode is not functional	X	X

2. Analog Front-End Controller (AFEC)

2.1 Write Protection Reference: M32DOC-497

The AFEC_CSELR register is not write-protected.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.2 Performance Reference: M32DOC-498

The AFEC is sensitive to noise. Too much noise may lead to reduced AFEC performance, especially INL, DNL and SNR. The following situations generate noise:

- Using a 64-pin QFP package option (it does not have the VREFN pin)
- Device activity (that is, clock tree)
- External components (that is, missing on-board supply decoupling capacitors)

Workaround

Adapt the environment to the expected level of performances.

Affected Silicon Revisions

A	B						
X	X						

2.3 AOFF bit Reference: TPUBSAMV-35

Changing the AOFF bit in the AFEC_COCCR register during conversions is not safe.

The recommended value of the AOFF bit is 512 (the default value is zero). Different values are possible for each channel. The AOFF bit is read and updated during the AFE start-up sequence and at the end of each conversion. If during AFE idle time (no conversion is on-going) the user updates the AOFF bit for the next channel to be converted, the next conversion will be incorrect.

Workaround

The value of the AOFF bit can be updated only if the AFEC module is restarted, or if two conversions are run; the second one will have the correct AOFF bit setting.

SAM E70/S70/V70/V71 Family

Analog Front-End Controller (AFEC)

Affected Silicon Revisions

A	B						
X	X						

3. ARM Cortex-M7

3.1 ARM® Cortex®-M7 Reference: M32DOC-499

All issues related to the ARM r0p1 (for MRLA) and r1p1 (and MRLB) cores are described on the ARM website.

Workaround

Refer to the following ARM documentation:

- For ARM Cortex-M7 r0p1 core (MRLA device): <https://silver.arm.com/download/download.tm?pv=2004343>
- For ARM Cortex-M7 r1p1 core (MRLB device): <https://silver.arm.com/download/download.tm?pv=3257391&p=1929427>
- ARM Embedded Trace Macrocell CoreSight ETM-M7 (TM975) Software Developers Errata Notice: <https://silver.arm.com/download/download.tm?pv=1998309>

Affected Silicon Revisions

A	B						
X	X						

4. Boundary Scan Mode

4.1 Internal Regulator Reference: M32DOC-500

The internal regulator is OFF in Boundary Scan mode.

Workaround

The user must provide external VDDCORE (1.2V) to perform Boundary Scan mode.

Affected Silicon Revisions

A	B						
X							

5. Device

5.1 AHB Peripheral (AHBP) Port Frequency Ratio Reference: M32DOC-501

Peripheral accesses done through the AHBP with a Core/Bus ratio of 1/3 and 1/4 may lead to unpredictable results.

Workaround

The user must use a Core/Bus frequency ratio of 1 or 1/2.

Affected Silicon Revisions

A	B						
X	X						

5.2 AHB Slave (AHBS) Port Latency Access Reference: M32DOC-502

DMA accesses done through the AHBS to the TCM with a Core/Bus ratio of 1/2, 1/3, and 1/4 may lead to latency due to one Wait state added to the access from the bus to AHBS.

Workaround

The user must use only the Core/Bus frequency ratio of 1 to guarantee the length of the access.

Affected Silicon Revisions

A	B						
X	X						

5.3 System Performance Reference: M32S-221

Very few applications have experienced uncorrelated system noise and clock jitter during SDRAM R/W access or PCK-based external clock operations. Inadequate power supply, decoupling, and less than robust PCB layout and manufacture process can further worsen this issue. These failures can occur across the full voltage and temperature range.

Workaround

Solid PCB power supply layout and decoupling can help mitigate such issues. It is recommended to use a 0.1µF decoupling capacitor with each power pin pair. The decoupling capacitors must be placed close to power pins. Careful attention to SDRAM board layout and line termination will significantly improve the performance. Refer to the “SAM E70/S70/V70/V71 Data Sheet”, (DS60001527), Section 60. “Schematic Checklist” for system recommendations, including SDRAM and line termination circuits implemented on the SAM E70 XULT board.

If devices still showing these behaviors or failure after following the above guidance, submit a technical support request. To submit a technical support request in Microchip’s technical support system, an active myMicrochip account is required. For additional information on how to submit a request, follow the link: <https://microchipsupport.force.com/s/article/How-to-submit-a-case>.

SAM E70/S70/V70/V71 Family

Device

Affected Silicon Revisions

A	B						
X	X						

6. Extended DMA Controller (XDMAC)

6.1 TCM Accesses Reference: M32DOC-503

If TCM accesses are generated through the AHBS port of the core, only 32-bit accesses are supported. Accesses that are not 32-bit aligned may overwrite bytes at the beginning and at the end of 32-bit words.

Workaround

The user application must use 32-bit aligned buffers and buffers with a size of a multiple of 4 bytes when transferring data to or from the TCM through the AHBS port of the core.

Affected Silicon Revisions

A	B						
X							

6.2 Byte and Half-Word Accesses Reference: M32DOC-506

If XDMAC is used to transfer 8-bit or 16-bit data in Fixed Source Address mode or Fixed Destination Address mode, source and destination addresses are incremented by 8-bit or 16-bit.

Workaround

The user can resolve this issue by setting the source and destination addressing mode to use microblock and data striding with microblock stride set to 0 and data stride set to -1.

Affected Silicon Revisions

A	B						
X	X						

6.3 Request Overflow Error Reference: M32DOC-509

When a DMA memory-to-memory transfer is performed, if the hardware request line selected by the field PERID bit in the XDMAC_CCx register toggles when the copy is enabled, the ROIS bit in the XDMAC_CISx register is set incorrectly. The memory transfer proceeds normally and the data area is correctly transferred.

Workaround

Configure the PERID bit to an unused peripheral ID.

Affected Silicon Revisions

A	B						
X	X						

7. Fast Flash Programming Interface (FFPI)

7.1 Flash Programming Reference: M32DOC-510

The FFPI programs only 1 MB of Flash memory.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

8. Ethernet MAC (GMAC)

8.1 Priority Queues Reference: M32DOC-535

On Revision A silicon, only three priority queues are available with the following sizes:

Queue Number	Queue Size
2 (highest priority)	4 KB
1	2 KB
0 (lowest priority)	2 KB

Workaround

None.

Affected Silicon Revisions

A	B						
X							

9. Inter-IC Sound Controller (I2SC)

9.1 Module Availability Reference: M32DOC-515

The Inter-IC Sound Controller (I2SC) is not available.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

9.2 Corrupted First Sent Data Reference: M32DOC-516

Immediately after the I2SC module is reset, the first data sent by the controller on the I2SDO line is corrupted. Any data that follows is not affected.

Workaround

None.

Affected Silicon Revisions

A	B						
	X						

10. Controller Area Network (MCAN)

10.1 Non-ISO Operation Reference: M32DOC-536

The default frame format on Revision A silicon does not match the default format specified in the current device data sheet.

Workaround

To retain Revision A behavior, set the MCAN_CCCR.NISO bit to '1'.

Affected Silicon Revisions

A	B						
X							

10.2 MCAN_CCCR Register Reference: M32DOC-537

In Revision A silicon, the MCAN CC Control register content does not match the content of the current device data sheet.

- NISO bit is missing
- EFBI bit is named FDBS
- PXHD bit is named FDO
- BRSE bit and FDOE bit are named CME[1:0]
- CMR[1:0] bits are present

Workaround

None.

Affected Silicon Revisions

A	B						
X							

10.3 Transmitter Delay Compensation Value (TDCV) Bits Reference: M32DOC-538

In Revision A silicon, the Transmitter Delay Compensation Value (TDCV) bit field does not match the content in the current device data sheet.

In Revision A silicon, the TDCV bits are located in the MCAN_TEST register.

In the current device data sheet, the TDCV bits are located in the MCAN_PSR register.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

10.4 MCAN_PSR Register Reference: M32DOC-539

In Revision A silicon, the content of the MCAN Protocol Status register differs from the content in the current device data sheet.

- PXE bit is not available
- RFDF bit is named REDL
- DLEC[2:0] bits are named FLEC[2:0]

Workaround

None.

Affected Silicon Revisions

A	B						
X							

10.5 MCAN_IR Register Reference: M32DOC-540

In Revision A silicon, the content of the MCAN Interrupt register differs from the content in the current device data sheet.

- STE and FOE bits are present
- ARA bit is replaced by the ACKE bit
- PED bit is replaced by the BE bit
- PEA bit is replaced by the CRCE bit

Workaround

None.

Affected Silicon Revisions

A	B						
X							

10.6 MCAN_IE Register Reference: M32DOC-541

On Revision A silicon, the content in the MCAN Interrupt Enable register does not match the content in the current device data sheet.

- STEE and FOEE bits are present
- ARAE bit is replaced by the ACKEE bit

- PEDE bit is replaced by the BEE bit
- PEAE bit is replaced by the CRCEE bit

Workaround

None.

Affected Silicon Revisions

A	B						
X							

10.7 MCAN_ILS Register Reference: M32DOC-542

On Revision A silicon, the content in the MCAN Interrupt Line Support Register does not match the content in the current device data sheet.

- STEL and FOEL bits are present
- ARAL bit is replaced by the ACKEL bit
- PEDL bit is replaced by the BEL bit
- PEAL bit is replaced by the CRCEL bit

Workaround

None.

Affected Silicon Revisions

A	B						
X							

10.8 MCAN Data Bit Timing and Prescaler Register Reference: M32DOC-543

On Revision A silicon, the MCAN Data Bit Timing and Prescaler register (MCAN_DBTP) is named MCAN Fast Bit Timing and Prescaler register (MCAN_FBTP).

Workaround

When using Revision A silicon, ensure that the name MCAN_FBTP is used.

Affected Silicon Revisions

A	B						
X							

10.9 MCAN Nominal Bit Timing and Prescaler Register Reference: M32DOC-544

On Revision A silicon, the MCAN Nominal Bit Timing and Prescaler register (MCAN_NBTP) is named MCAN Bit Timing and Prescaler register (MCAN_BTP).

SAM E70/S70/V70/V71 Family

Controller Area Network (MCAN)

Workaround

When using Revision A silicon, ensure that the name MCAN_BTP is used.

Affected Silicon Revisions

A	B						
X							

10.10 MCAN Transmitter Delay Compensation Register Reference: M32DOC-545

In Revision A silicon, the MCAN Transmitter Delay Compensation Register (MCAN_TDCR) does not exist.

Workaround

The transmit delay compensation offset is configured in the TDCO field of the MCAN_FBTP register.

Affected Silicon Revisions

A	B						
X							

10.11 Timestamping Function Reference: M32DOC-546

On Revision A silicon, TC Counter 0 is not connected to PCK6 and PCK7; therefore, the timestamping functionality does not exist.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

11. Parallel Input/Output (PIO)

11.1 PIO Line Configuration for AFEC and DACC Analog Inputs Reference: MC32DOC-517

To enable the analog inputs, AFE_ADx or DACx, the pull-up resistors on the I/O lines must be disabled in the PIO user interface prior to writing registers AFEC_CHER or DACC_CHER.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

12. Power Management Controller (PMC)

12.1 Wait Mode Exit Fail from Flash Reference: M32DOC-518

The delay to exit from Wait mode is too short to respect the Flash wake-up time from Stand-by mode and Deep Power-Down mode. This delay may lead to bad opcode fetching.

Workaround 1

Use the Flash in Idle mode (FLPM = 2).

Workaround 2

If Flash in Stand-by mode (FLPM = 0) or in Deep Power-Down mode (FLPM = 1) is used, run the wake-up routine from SRAM. This option provides a slight improvement in power consumption.

Affected Silicon Revisions

A	B						
X	X						

12.2 PMC_OCR Register Calibration Reporting Reference: M32DOC-519

When reading the PMC_OCR register with the SEL8 and SEL12 bits cleared, the CAL8 and CAL12 bits are not updated with the manufacturing calibration bits of the Main RC Oscillator. However, the Main RC Oscillator is loaded with this manufacturing calibration data.

Workaround

To recover the manufacturing calibration bits of the Main RC oscillator, use the following steps:

1. Execute the 'Get CALIB Bit' command by writing the FCMD bit in the EEFC_FCR register with the GCALB command.
2. Read the EEFC_FRR register. The 8 MHz RC calibration bits are EEFC_FRR bits [17-11] and the 12 MHz RC calibration bits are EEFC_FRR bits [25-19].

Affected Silicon Revisions

A	B						
X	X						

13. Quad Serial Peripheral Interface (QSPI)

13.1 Module Hangs with Long DLYCS Reference: M32DOC-520

The QSPI module hangs if a command is written to any QSPI register during the delay defined in the DLYCS bit. There is no status bit to flag the end of the delay.

Workaround

The DLYCS bit defines a minimum period over which the Chip Select is deasserted, which is required by some memories. This delay is generally less than 60 ns and comprises internal execution time, arbitration, and latencies. Therefore, the DLYCS bit must be configured to be slightly higher than the value specified for the slave device. The software must wait for at least this same period of time before a command can be written to the QSPI module.

Affected Silicon Revisions

A	B						
X	X						

13.2 WDRBT Reference: M32DOC-592

When the QSPI is configured in SPI mode, the Wait Data Read Before Transfer (WDRBT) feature does not work.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

14. Real-Time Clock (RTC)

14.1 RTC_CALR Reset Value Reference: M32DOC-521

On Revision A silicon, the reset value of the RTC_CALR register is 0x01E11220.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

15. SDRAM Controller (SDRAMC)

15.1 SDRAM Controller Scrambling Use Limitation Reference: M32DOC-522

The scrambling or unscrambling feature of the SDRAM Controller (SDRAMC) has a use limitation.

Workaround

The read of a scrambled area must be performed with the same type of access done during the write of this area. It is recommended to read and write using 32-bit words.

Affected Silicon Revisions

A	B						
X							

15.2 USB and SDRAM Concurrent Access Issue Reference: M32DOC-568

USB module functionality is adversely affected with concurrent SDRAM access.

Workaround

Ensure that no concurrent module operations when using both SDRAM and USB.

Affected Silicon Revisions

A	B						
X	X						

15.3 Operational Voltage Reference: M32S-200

The SDRAM operation at 1.8 Vdc is not supported. The recommended operational voltage is 3.3 Vdc +/-10%.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

16. Static Memory Controller (SMC)

16.1 SMC_WPSR Register Write Protection Reference: M32DOC-523

When the write protection feature is enabled and a write attempt into a protected register is performed, the Write Protection Violation Source (WPVSR) bit field in the SMC_WPSR register does not report the right violation source. As a consequence, the value in the WPVSR bit field is incorrect. This issue does not affect the write protection feature itself, which is fully functional.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

17. Serial Synchronous Controller (SSC)

17.1 Inverted Left/Right Channels Reference: M32DOC-524

When the SSC is in Slave mode, the TF signal is derived from the codec and not controlled by the SSC. The SSC transmits the data when detecting the falling edge on the TF signal after the SSC transmission is enabled. In some cases of overflow, a left/right channel inversion may occur. When this occurs, the SSC must be reinitialized.

Workaround

Using the SSC in Master mode will ensure that TF is controlled by the SSC and no error occurs. If the SSC must be used in TF Slave mode, the SSC must be started by writing TXEN and RXEN synchronously with the TXSYN flag rising in the SSC_SR.

Affected Silicon Revisions

A	B						
X							

17.2 Unexpected TD Output Delay Reference: M32DOC-525

An unexpected delay on TD output may occur when the SSC is configured with the following conditions:

- The START bit in the RCMR register = Start on falling edge/Start on Rising edge/Start on any edge
- The FSOS bit in the RFMR register = None (input)
- The START bit in the TCMR register = Receive Start

Under these conditions, an unexpected delay of two or three system clock cycles is added to the TD output.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

18. Supply Controller (SUPC)

18.1 Write-Protection Reference: M32DOC-526

The SUPC_WUIR register is not write-protected.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

18.2 Programmable Clock Controller Reference: M32VAL-5836

Programmable Clock Outputs, PCK0 and PCK2, selected from the clock generator outputs to drive the device PCK pins are not supported and should not be used.

Workaround

Use PCK1.

Table 18-1. Affected Silicon Revisions

A	B						
X	X						

19. TWI High-Speed (TWIHS)

19.1 I²C Hold Timing Incompatibility Reference: M32DOC-527

The TWIHS module is not compatible with I²C hold timing. The divider to program the hold time is too short to achieve the expected hold time at high frequency. The achieved time is 227 ns maximum at 150 MHz, instead of the required 300 ns.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

19.2 Clear Command Reference: M32DOC-528

A bus reset using the CLEAR bit of the TWIHS Control register does not work correctly during a bus busy state.

Workaround

Reconfigure the TWCK line in GPIO output and generate nine clock pulses through software to unlock the I²C device.

After that the TWCK line can be reconfigured as a peripheral line.

Affected Silicon Revisions

A	B						
X							

20. Universal Synchronous Asynchronous Receiver Transmitter (USART)

20.1 Flow Control with DMA Reference: M32DOC-529

The CTS and RTS signals are not connected to DMA. Therefore, when DMA is used, Flow Control is not supported.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

20.2 Bad Frame Detection Reference: M32DOC-530

If a bad frame is received (i.e., incorrect baud rate) with the last data bit being sampled at 1, frame error detection does not occur.

Workaround

There is no general workaround. When performing baud rate detection with receive part, the transmit frame must be sent with a parity bit set to '0'.

Affected Silicon Revisions

A	B						
X	X						

21. USB High-Speed (USBHS)

21.1 USBHS Host Does Not Function in Low-Speed Mode Reference: M32DOC-531

The USB Host does not function in Low-Speed mode.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

21.2 64-pin LQFP Package Reference: M32DOC-532

The USBHS module does not function in 64-pin LQFP package devices.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

21.3 NO DMA for Endpoint 7 Reference: M32DOC-533

The DMA feature is not available for Pipe/Endpoint 7.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

22. Digital to Analog Converter Controller (DACC)

22.1 Interpolation Mode Reference: BUG300

The Interpolation mode that allows Oversampling Ratio (OSR) of 2x, 4x, 8x, 16x, or 32x is not functional.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

23. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001527C):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

23.1 Controller Area Network (MCAN)

The MCAN_CREL register reset value documented in the data sheet is applicable to devices with silicon revision B. The MCAN_CREL register reset value for devices with silicon revision A is 0x30130506.

23.2 Quad Serial Peripheral Interface (QSPI)

The QSPI in SPI mode does not support the *Wait Data Read Before Transfer* feature, the WDRBT bit in the SPI Mode Register (SPI_MR) must be ignored.

24. Appendix A: Revision History

Revision D (5/2019)

Updated the [Silicon Issue Summary](#) table to be more readable.

The following Silicon Issues were updated:

- [Boundary Scan Mode: Internal Regulator](#)
- [XDMAC: TCM Accesses](#)
- [FFPI: Flash Programming](#)
- [PMC: Wait Mode Exit Fail from Flash](#)
- [SDRAMC: SDRAM Controller Scrambling Use Limitation](#)
- [SMC: SMC_WPSR Register Write Protection](#)
- [TWIHS: I²C Hold Timing Incompatibility](#)
- [TWIHS: Clear Command](#)

The following Silicon Issues were added:

- [DEVICE: System Performance](#)
- [SDRAMC: Operational Voltage](#)

Revision C (11/2018)

The following Silicon Issues were added:

- 18.2 [Programmable Clock Controller](#)
- 22.1 [Interpolation Mode](#)

The following Data Sheet Clarifications were added:

- [Controller Area Network \(MCAN\)](#)
- [Quad Serial Peripheral Interface \(QSPI\)](#)

Revision B (8/2018)

This revision was updated for Revision B silicon.

The following Silicon Issue was added:

- 13.2 [WDRBT](#)

Revision A (11/2017)

Initial release of this document.

The Microchip Web Site

Microchip provides online support via our web site at <http://www.microchip.com/>. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at <http://www.microchip.com/>. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://www.microchip.com/support>

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KeeLoq, KeeLoq logo, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-4538-8

Quality Management System Certified by DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/support Web Address: www.microchip.com	Asia Pacific Office Suites 3707-14, 37th Floor Tower 6, The Gateway Harbour City, Kowloon Hong Kong Tel: 852-2943-5100 Fax: 852-2401-3431 Australia - Sydney Tel: 61-2-9868-6733 Fax: 61-2-9868-6755 China - Beijing Tel: 86-10-8569-7000 Fax: 86-10-8528-2104 China - Chengdu Tel: 86-28-8665-5511 Fax: 86-28-8665-7889 China - Chongqing Tel: 86-23-8980-9588 Fax: 86-23-8980-9500 China - Dongguan Tel: 86-769-8702-9880 China - Guangzhou Tel: 86-20-8755-0029 China - Hangzhou Tel: 86-571-8792-8115 Fax: 86-571-8792-8116 China - Hong Kong SAR Tel: 852-2943-5100 Fax: 852-2401-3431 China - Nanjing Tel: 86-25-8473-2460 Fax: 86-25-8473-2470 China - Qingdao Tel: 86-532-8502-7355 Fax: 86-532-8502-7205 China - Shanghai Tel: 86-21-3326-8000 Fax: 86-21-3326-8021 China - Shenyang Tel: 86-24-2334-2829 Fax: 86-24-2334-2393 China - Shenzhen Tel: 86-755-8864-2200 Fax: 86-755-8203-1760 China - Wuhan Tel: 86-27-5980-5300 Fax: 86-27-5980-5118 China - Xian Tel: 86-29-8833-7252 Fax: 86-29-8833-7256	China - Xiamen Tel: 86-592-2388138 Fax: 86-592-2388130 China - Zhuhai Tel: 86-756-3210040 Fax: 86-756-3210049 India - Bangalore Tel: 91-80-3090-4444 Fax: 91-80-3090-4123 India - New Delhi Tel: 91-11-4160-8631 Fax: 91-11-4160-8632 India - Pune Tel: 91-20-3019-1500 Japan - Osaka Tel: 81-6-6152-7160 Fax: 81-6-6152-9310 Japan - Tokyo Tel: 81-3-6880-3770 Fax: 81-3-6880-3771 Korea - Daegu Tel: 82-53-744-4301 Fax: 82-53-744-4302 Korea - Seoul Tel: 82-2-554-7200 Fax: 82-2-558-5932 or 82-2-558-5934 Malaysia - Kuala Lumpur Tel: 60-3-6201-9857 Fax: 60-3-6201-9859 Malaysia - Penang Tel: 60-4-227-8870 Fax: 60-4-227-4068 Philippines - Manila Tel: 63-2-634-9065 Fax: 63-2-634-9069 Singapore Tel: 65-6334-8870 Fax: 65-6334-8850 Taiwan - Hsin Chu Tel: 886-3-5778-366 Fax: 886-3-5770-955 Taiwan - Kaohsiung Tel: 886-7-213-7830 Taiwan - Taipei Tel: 886-2-2508-8600 Fax: 886-2-2508-0102 Thailand - Bangkok Tel: 66-2-694-1351 Fax: 66-2-694-1350	Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 Denmark - Copenhagen Tel: 45-4450-2828 Fax: 45-4485-2829 Finland - Espoo Tel: 358-9-4520-820 France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 France - Saint Cloud Tel: 33-1-30-60-70-00 Germany - Garching Tel: 49-8931-9700 Germany - Haan Tel: 49-2129-3766400 Germany - Heilbronn Tel: 49-7131-67-3636 Germany - Karlsruhe Tel: 49-721-625370 Germany - Munich Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 Germany - Rosenheim Tel: 49-8031-354-560 Israel - Ra'anana Tel: 972-9-744-7705 Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781 Italy - Padova Tel: 39-049-7625286 Netherlands - Drunen Tel: 31-416-690399 Fax: 31-416-690340 Norway - Trondheim Tel: 47-7289-7561 Poland - Warsaw Tel: 48-22-3325737 Romania - Bucharest Tel: 40-21-407-87-50 Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 Sweden - Gothenberg Tel: 46-31-704-60-40 Sweden - Stockholm Tel: 46-8-5090-4654 UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820